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10/768,401	01/30/2004	Michele Borgatti	02AG38953426	3793

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/768,401	BORGATTI ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12,14-17,19-22,24-26,28-31.33-35* is/are rejected.

7)☒ Claim(s) *13,18,23,27,32 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10,11,14,17, are rejected under 35 U.S.C. 103(a) as being unpatentable over of Bocchi (patent No. 6,845,276)(cited in the last office action) in view of Brown (IEEE article entitled FPGA and CPLD Architectures: A tutorial) in view of Iwata (patent No. 6,662,314)(cited in last office action).

3. Bocchi taught the invention substantially as claimed including a data processing "DP") system comprising: (as per claims 10,):

4. a) Processing unit (10) (e.g., see fig. 1) comprising microprocessor (66) embedded flash memory (62) for non-volatile storage of code, and data (e.g., see col. 5, lines 5-25) comprising a FPGA port (e.g., see fig. 1), direct memory access channel route between Flash memory and FPGA or SRAM via CPLD), connected to a field programmable gate array (64) and the SRAM (68) , direct memory access channel comprising and interface (CPLD) connected to a FPGA port and a port of the flash memory (62) (e.g., see fig. 1). Bocchi did not expressly detail that the FPGA was an SRAM embedded FPGA. Brown taught that FPGA embedded FPGAs where SRAM emedded FPGA are programmable (e.g., see page 53, column 1 and table1 on page 45) and the FPGA current commercial products (as of summer 1996) use either SRAM

or antifiuse technologies (e.g., see page 45, col. 1). Since SRAM was commercially available and reprogrammable one of ordinary skill would have been motivated to utilized SRAM for the FPGA (e.g., see col. 10, lines 14-25).

5. One of ordinary skill would have been motivated to incorporate the teachings of of Bocchi and Brown. Both references were directed toward the problems of implementing systems using CPLD and FPGA and SRAMs. One of ordinary skill would have been motivated to incorporate the Bocchi teachings of the commercially available FPGA technologies along with the capabilities of each at least to provide for the low cost quick and efficient implementation of the Bocchi teachings.

6. As per claims 10, Bocchi did not expressly detail that SRAM (6) embedded FPGA, CPU, controller and Flash memory all integrated on a single chip. Iwata taught this limitation with the microprocessor (CPU 3) embedded flash memory (5) for non-volatile storage of code, and data (e.g., see col. 10, line 53-col. 11, line 20) comprising a port, direct memory access channel (7) controllers (7,8), SRAM (6) all integrated on a single chip (e.g., see fig. 1 and col. 4, lines 46-63).

7. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Bocchi and Iwata. One of ordinary skill would have been motivated to incorporate the Iwata teaching of placing the CPU, SRAM , Flash , Controller on the same chip into the Bochhi system to reduce system size and cost.

8. Bocchi taught the CPLD operated as a Direct memory access channel and the FPGA was connected to the FPGA port of the flash memory through the CPLD (that comprised that operated as a DMA channel) (e.g., see fig. 1, and col. 4, line 51-col. 5,

line 32)[the CPLD performs interfacing with memory even when CPU is disabled (e.g., see col. 9, line 55-col. 10, line 28].

9. On the other hand, one of ordinary skill would have connected the FPGA port and the FPGA interface to the DMA port to at least to provide a means to load the Flash memory from external memory such as from the host's memory.

10. As to the limitations of claim 11, Bocchi taught the flash memory having a data port (connected to data bus e.g., see fig. 1) and code port (e.g., see fig. 1). Further Iwata taught each DMA channel comprised a DMA controller (e.g., see col. 4 lines 46-63). Therefore it would have been obvious to one of ordinary skill that the DMA channel of Iwata was able to handle transfers of streams of bits while the microprocessor performed other operations including fetching data and instructions from the SRAM or Flash memory bus (9) (e.g., see fig. 1)(e.g., see col. 1, line 55-col. 2, line 53).

11. As to claims 14, Bocchi taught the code port of the embedded Flash memory is for optimizing random access time [at least in that separate code and data ports allow concurrent transfer of code and data] and an application system supported by the reconfigurable processing unit[the processor allows for an application to be processed by an optimized system that is reconfigured to the application]; the data port of the embedded Flash memory is for allowing access to application data for modification thereof[the data port of the flash memory is connected to data bus and CPU for processing and modification of data] ; and the FPGA port of the embedded Flash memory is for providing serial access for downloading the bit streams for an embedded FPGA configuration (e.g., see fig. 1).

12. As per claim 17, Iwata taught a system bus connected to the DMA channel (7) and the embedded flash memory (5) e.g., see fig. 1).

13. Claims 19,21,24,28,30,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Bocchi (patent No. 6,845,276) in view of Brown (IEEE article entitled FPGA and CPLD Architectures: A tutorial).

14. Bocchi taught the invention substantially as claimed including a data processing "DP") system comprising: (as per claims 19,20,21,28,29,30):

15. a) Processing unit (10) (e.g., see fig. 1) comprising microprocessor (66) embedded flash memory (62) for non-volatile storage of code, and data (e.g., see col. 5, lines 5-25) comprising a FPGA port (e.g., see fig. 1), direct memory access channel (route between Flash memory and FPGA or SRAM via CPLD), connected to a field programmable gate array (64) and the SRAM (68) , direct memory access channel comprising and interface (CPLD) connected to a FPGA port and a port of the flash memory (62) (e.g., see fig. 1). Bocchi did not expressly detail that the FPGA was an SRAM embedded FPGA. Brown taught that FPGA embedded FPGAs where SRAM emedded FPGA are programmable (e.g., see page 53, column 1 and table1 on page 45) and the FPGA current commercial products (as of summer 1996) use either SRAM or antifiuse technologies (e.g., see page 45, col. 1). Since SRAM was commercially available and reprogrammable one of ordinary skill would have been motivated to utilized SRAM for the FPGA (e.g., see col. 10,lines 14-25 of Bocchi).

16. One of ordinary skill would have been motivated to incorporate the teachings of of Bocchi and Brown. Both references were directed toward the problems of implementing systems using CPLD and FPGA and SRAMs. One of ordinary skill would have been motivated to incorporate the Bocchi teachings of the commercially available FPGA technologies along with the capabilities of each at least to provide for the low cost and quick implementation of the Bocchi teachings.

17. Bocchi taught the CPLD operated as a Direct memory access channel and the FPGA was connected to the FPGA port of the flash memory through the CPLD (that comprised that operated as a DMA channel) (e.g., see fig. 1, and col. 4, line 51-col. 5, line 32)[the CPLD performs interfacing with memory even when CPU is disabled (e.g., see col. 9, line 55-col. 10, line 28].

18. On the other hand, one of ordinary skill would have connected the FPGA port and the FPGA interface to the DMA port to at least to provide a means to load the Flash memory from external memory such as from the host's memory.

19. Bocchi taught the flash memory having a data port (connected to data bus e.g., see fig. 1) and code port (e.g., see fig. 1). Further Iwata taught each DMA channel comprised a DMA controller (e.g., see col. 4 lines 46-63). Therefore it would have been obvious to one of ordinary skill that the DMA channel of Iwata was able to handle transfers of streams of bits while the microprocessor performed other operations including fetching data and instructions from the SRAM or Flash memory bus (9) (e.g., see fig. 1)(e.g., see col. 1, line 55-col. 2, line 53).

20. As to claims 24,33 Bocchi taught the code port of the embedded Flash memory is for optimizing random access time [at least in that separate code and data ports allow concurrent transfer of code and data] and an application system supported by the reconfigurable processing unit[the processor allows for an application to be processed by an optimized system that is reconfigured to the application]; the data port of the embedded Flash memory is for allowing access to application data for modification thereof[the data port of the flash memory is connected to data bus and CPU for processing and modification of data] ; and the FPGA port of the embedded Flash memory is for providing serial access for downloading the bit streams for an embedded FPGA configuration (e.g., see fig. 1).

21. Claims 20,29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bocchi and Brown as applied to claims 19, 28 above, and further in view of Iwata (patent No. 6,662,314).

22. As per claims 20,29, Bocchi did not expressly detail that SRAM (6) embedded FPGA, CPU, controller and Flash memory all integrated on a single chip. Iwata taught this limitation with the microprocessor (CPU 3) embedded flash memory (5) for non-volatile storage of code, and data (e.g., see col. 10, line 53-col. 11, line 20) comprising a port, direct memory access channel (7) controllers (7,8), SRAM (6) all integrated on a single chip (e.g., see fig. 1 and col. 4, lines 46-63).

23. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Bocchi and Iwata. One of ordinary skill would have been motivated to

incorporate the Iwata teaching of placing the CPU, SRAM , Flash , Controller on the same chip into the Bochhi system to reduce system size and cost.

24. Claims 12, is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata,Brown and Bocchi as applied to claims 10,11, above, and further in view of Stancil and Kuo (both cited in the last office action).

25. Stancil taught a flash memory (204,308)comprising a modular array on N modules and power memory arbiter (304) (e.g., see fig. 3)

26. As per claim 12, Stancil taught the Flash memory (e.g., see col. 8,lines 19-37) comprising modular array of memory modules (e.g., col. 7, line 12-col. 8,line 57). Also Kuo taught a flash memory comprising a charge pump (38) (e.g., fig. 3 and paragraph [0026]).

27. It would have been obvious to one of ordinary skill to combine the teachings of Iwata and Stancil. Both references were directed to the problems of systems that use embedded flash memories. One ordinary skill in the DP art would have been motivated to incorporate the arbiter to provide better communication between the flash memory and a plurality of system components.

28. It would have been obvious to one of ordinary skill to combine the teachings of Iwata and Kuo. Both references were directed to the problems of systems that use embedded flash memories. One of ordinary skill would have been motivated to incorporate the charge pump of Kuo at least to stabilize voltage levels when a flash

memory is embedded on a chip with other elements (e.g. see paragraphs 0010-0015 of Kuo).

29. Claims 22,31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown and Bocchi as applied to claims 19-21,24,28-30,33 above, and further in view of Stancil and Kuo (both cited in the last office action).

30. Stancil taught a flash memory (204,308)comprising a modular array on N modules and power memory arbiter (304) (e.g., see fig. 3)

31. As per claims 22,31 Stancil taught the Flash memory (e.g., see col. 8,lines 19-37) comprising modular array of memory modules (e.g., col. 7, line 12-col. 8,line 57). Also Kuo taught a flash memory comprising a charge pump (38) (e.g., fig. 3 and paragraph [0026]).

32. It would have been obvious to one of ordinary skill to combine the teachings of Bocchi and Stancil. Both references were directed to the problems of systems that use embedded flash memories. One ordinary skill in the DP art would have been motivated to incorporate the arbiter to provide better communication between the flash memory and a plurality of system components.

33. It would have been obvious to one of ordinary skill to combine the teachings of Bocchi and Kuo. Both references were directed to the problems of systems that use embedded flash memories. One of ordinary skill would have been motivated to incorporate the charge pump of Kuo at least to stabilize voltage levels when a flash

memory is embedded on a chip with other elements (e.g. see paragraphs 0010-0015 of Kuo).

34. Claims 15,16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata, Brown and Bocchi and Brown as applied to claims 10,11,14, above, and further in view of Blemel (patent No. 6, 938,177)(cited in the last office action).

35. Blemel taught a EEPROM of Flash memory for programming a FPGA (e.g., see col. 3, lines 1-25). Therefore one of ordinary skill would have been motivated to provide plural registers for input and output to/from the FLASH memory to adjust for the speed difference between the processing portion and the memory portion of the system.

36. It would have been obvious to one of ordinary skill to combine the teachings of Iwata and. Blemel. Both references were directed to the problems of systems that use embedded flash memories. One of ordinary skill would have been motivated to add the Blemel FPGA to provide reconfigurable processing to optimize processing of applications.

37. As to the use of a chip select and burst enable signal (claim 16) the use of these signals to access memory was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to access data using serial and burst access depending on the speed requirements of the transmission of data.

38. Claims 25,26,34,35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown and Bocchi as applied to claims 19-21,24,28-30,33 above, and further in view of Blemel (patent No. 6, 938,177)(cited in the last office action).

39. Blemel taught a EEPROM of Flash memory for programming a FPGA (e.g., see col. 3, lines 1-25). Therefore one of ordinary skill would have been motivated to provide plural registers for input and output to/from the FLASH memory to adjust for the speed difference between the processing portion and the memory portion of the system.

40. It would have been obvious to one of ordinary skill to combine the teachings of Bocchi and. Blemel. Both references were directed to the problems of systems that use embedded flash memories. One of ordinary skill would have been motivated to add the Blemel FPGA to provide reconfigurable processing to optimize processing of applications.

41. As to the use of a chip select and burst enable signal (claim 16) the use of these signals to access memory was well known in the art at the time of the claimed invention. Therefore one of ordinary skill would have been motivated to access data using serial and burst access depending on the speed requirements of the transmission of data.

Allowable Subject Matter

42. Claims 13,18,23,27,32,36, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 10-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Quicklogic taught the popular technologies comprising SRAM and a benefit to using SRAM FPGAS is that they are reprogrammable (e.g., see pp.1, 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER